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PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appellants:	Behrens et al.
Serial No.:	10/032,513
For:	DATA FLOW SYNCHRONIZATION
Filed:	26 OCT 2001
Examiner:	Juan A. Torres
Art Unit:	2611
Confirmation No.:	6890
Customer No.:	27,623

Attorney Docket Nos.: 20 01 0631
0003012USU/3154

REPLY BRIEF (37 C.F.R. 41.41)

Mail Stop Appeal Brief – Patents
Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

On 12 APR 2007, Appellants filed an Appeal Brief for the above-noted application. On 14 JUN 2007, the Office mailed an Examiner's Answer. Appellants are submitting the present Reply Brief in response to the Examiner's Answer.

This Reply Brief is being filed in accordance with the provisions of 37 C.F.R. 41.41. The Examiner's Answer does not raise any new grounds of rejection of the claims, however the Examiner does raise new points of argument. This brief is directed only to the new points of argument.

Claims 1 – 11 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,324,664 to Farwell et al. (hereinafter "the Farwell et al. patent") in view of U.S. Patent No. 6,055,285 to Alston (hereinafter "the Alston patent").

Point 1

In the Appeal Brief, near the bottom of page 8, Appellants argue that if the Farwell et al. patent were modified to include the synchronization circuit of the Alston patent, such a modification would obviate the manner in which modulo counter 27 and test bus controller 29 coordinate the writing of data to, and reading of data from, output memory 25, thus changing the principle of operation of the Farwell et al. patent.

In response, the Examiner's Answer, on page 11, presents the following argument:

> The Examiner disagrees, and asserts, that, as indicated in the previous Office action, Farwell doesn't specifically disclose the details that the first clock signal controls a write access onto the buffer; and that the second control signal controls a read access onto the buffer, for this reason the Examiner uses a second reference that provides the details of how to transfer information between a first clock domain to a second clock domain, where the first clock domain and the second clock domain are mutually asynchronous, Farwell (11-2001) patent doesn't provide these details. This doesn't change any principle of operation, Alston (4-2000) simply provide the details of one method of how to produce the transfer of these data between two different clock domains that are asynchronous (emphasis in original).

Appellants respectfully disagree with the Examiner's assertion that the cited combination of the Farwell et al and Alston patents would not change the principle of operation of the Farwell et al. patent.

In the Farwell et al. patent, a system clock (SYSCLK) clocks a modulo counter 27 and a scan path 20 (see FIG. 1), and a test bus controller 29 provides a TEST CLOCK to a read/write controller 19 (col. 4, lines 6 - 8). Read/write controller 19 (i) evaluates an index provided by modulo counter 27 to enable output memory 25 to sample the output of scan path

20, i.e., to write data into output memory 25, and (ii) in cooperation with test bus controller 29[1] reads output memory 25 (col. 3, line 65 - col. 4, line 8; and col. 4, lines 25 – 45).

In the Alston patent, with reference to FIG. 2, describes a FIFO buffer 200 that includes a first synchronization circuit 210 and a second synchronization circuit 212 (col. 8, lines 57 – 62). First synchronization circuit 210 generates a synchronized write address pointer (SYNCHED WRITE POINTER) on a synchronized write pointer bus 214, which is provided as an input to a read controller 142 (col. 8, lines 62 – 66). Second synchronization circuit 212 generates a synchronized read address pointer (SYNCHED READ POINTER) on a synchronized read pointer bus 216, which is provided as an input to a write controller 140 (col. 9, lines 4 – 7).

The Examiner has not expressly stated how the Farwell et al. patent could be modified to include the circuitry of the Alston patent, but on page 4 of the Reply Brief states that it would have been obvious to supplement the apparatus for testing disclosed by the Farwell et al. patent with the synchronization circuit disclosed by the Alston patent. However, Appellants believe that a modification of the circuit of the Farwell et al. patent to include the first synchronization circuit 210 and the second synchronization circuit 212 of the Alston patent (either by replacing or supplementing some component(s) of the Farwell et al. patent) would (a) obviate the need for the modulo counter 27 of the Farwell et al. patent to provide the index, and (b) obviate the manner in which read/write controller 19 evaluates the index and coordinates the writing of data to, and reading of data from, output memory 25. Accordingly, Appellants are maintaining that such a modification would change the principle of operation of the Farwell et al. patent.

Point 2

In the Appeal Brief, near the bottom of page 8, Appellants argue that whereas the Farwell et al. patent expressly states that the system accommodates asynchronous clocks, there is no apparent need to modify the Farwell et al. patent to include the synchronization

[1] The Farwell et al. patent, at col. 4, line 44, refers to "test bus controller 27", but from FIG.1, it is clear that the Farwell et al. patent intended to refer to "test bus controller 29."

circuit of the Alston patent. In other words, Appellants are asserting that there is no motivation to combine the references.

In response, the Examiner's Answer, on page 12, presents the following argument.

> In this case, the motivation used is from the secondary reference...[and the] suggestion/motivation for doing so would have been synchronizing the transfer of data from a transmitting circuit operating in first clock domain to a receiving circuit operating in a second clock domain, where the first clock domain and the second clock domain are mutually asynchronous (Alston abstract and column 4 lines 14 – 24) (emphasis in original).

From the statement above, it appears that the Examiner is asserting that since the Alston patent presents a solution to a problem involving asynchronous clocks, the Alston patent also provides a motive to incorporate the solution into the system of the Farwell et al. patent. Appellants respectfully disagree.

The system in the Farwell et al. patent accommodates asynchronous clocks (col. 5, lines 33 – 38), and therefore addresses the problem of asynchronous clocks. Thus, the Farwell et al. patent has no need for the solution presented in the Alston patent.

Appellants submit that whereas the Farwell et al. patent has no need for the solution presented by the Alston patent, there is no motive to employ the solution presented by the Alston patent in the system of the Farwell et al. patent. Accordingly, Appellants are maintaining that there is no motivation to combine the Farwell et al. and Alston patents.

Point 3

Page 12 of the Examiner's Answer, includes the following statement:

> In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references.

Appellants are not sure of why the Examiner's Answer includes the above-noted statement. Appellants are not attaching the references individually. Appellants are asserting that (a) a modification of the Farwell et al. patent to include the synchronization circuit of the Alston patent would change the principle of operation of the Farwell et al. patent, and (b) there is no motive to combine the Farwell et al. and Alston patents. Thus, Appellants respectfully submit that the claims of the present application are patentable over the cited combination of the Farwell et al. and Alston patents.

In summary, Appellants are requesting that the Board of Appeals reverse the rejection of the claims, thereby enabling all of the pending claims to be allowed.

Respectfully submitted,

8/10/07
Date

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